Progress and challenges in building evolvable devices

Adrian Stoica, Ricardo Zebulum, and Didier Keymeulen
Jet Propulsion Laboratory
California Institute of Technology
4800 Oak Grove Drive
Pasadena, CA 91109
adrian.stoica@jpl.nasa.gov

Abstract

This paper presents JPL progress in building evolution-oriented reconfigurable devices. It surveys the FPTA family, and presents details of the latest chip, FPTA2, an array of 64 reconfigurable cells that can implement mixed-signal functions, include programmable capacitors and resistors and integrate photodetectors as part of a built-in vision sensor. The chip was fabricated in 0.18 micron CMOS. The paper also discusses some of the challenges in building such chips, as well as lessons learned while evolving circuits.

1. Introduction

The lack of suitable platforms for evolvable hardware (EHW) has been a concern of the field, especially since the chip first used for intrinsic experiments, the Xilinx 6216 has been out of the fabrication. Several research laboratories have embarked into an effort of building their own platforms, that includes board level solutions such as those developed at U. of Sussex [1] and Catholic University of Rio [2], or dedicated chips as pursued at JPL and Heidelberg University [3]. The JPL effort toward developing evolution-oriented devices stems from a set of requirements outlined in [4]. The approach for evolution-oriented chips initiated at JPL (and also used by the Heidelberg University, with a different cell design) was to allow reconfigurability at transistor level, building programmable transistor arrays (PTAs) that would allow synthesis of both analog and digital circuits. The first PTA was described in [5], [6] and relied on a cell with 8 transistors interconnected by 24 switches. The PTA chip was used to demonstrate intrinsic evolution of a variety of circuits, including logical gates, transconductance amplifiers, computational circuits, etc. It also demonstrated its value in generating new concepts such as mixtrinsic evolution [7], polymorphic electronics [8], repairing faulty circuits [9], and allowing the demonstration that evolvable hardware can expand the operational envelope of electronics at extreme temperatures [10], etc. The PTA chip included only 3 cells, inter-connectable but only through exterior wiring. The next chip in the family was the FPTA1, a proper field programmable transistor array with 12 cells. The main advantage of the FPTA1, besides the larger number of cells, was the fact that the chip included capacitors, which allowed its use in filter experiments, such as noise canceling. In many respects, the FPTA1 was a test/prototyping device for the FPTA2, the chip presented in more detail in this paper. The FPTA2 is a second generation evolution-oriented device, not only by level of integration, and incorporation of programmable resistors and capacitors, but most importantly because it includes a (vision) sensor array, realizing in fact the first evolvable sensor system on a chip. It is also in true sense a member of a new family, the field programmable mixed-signal arrays (FPMA), with the power of building complete analog circuits including amplifiers, filters, etc, as well as digital designs.

Section 2 presents FPTA2 details. Section 3 presents some lessons learned during the design of the FPTA family.

2. FPTA2: An evolvable system on a chip

FPTA2 is a second generation reconfigurable mixed signal array chip whose cells can be programmed at the transistor level. The chip architecture consists of an 8x8 matrix of re-configurable cells (Figure 1). The chip can receive 96 analog/digital inputs and provide 64 analog/digital outputs. Each cell is programmed through a 16 bits data bus/9 bits address bus control logic, which provides an addressing mechanism to download the bitstring of each cell. A total of 5000 bits is used to program the whole chip. The pattern of interconnection between cells is illustrated at the right of the figure, and shows how each cell interconnects with its north, south, east and west neighbors. An array of 16x8 photodetectors, distributed within the cells, is also integrated on chip. It is the first chip integrating reconfigurable processing circuitry with sensing. It is the first mixed-signal programmable array, FPMA; compared with FPAAs it can configure more Operational Amplifiers (OpAmps) than any commercial Field Programmable Analog Array (FPAA) chip (the largest commercial FPAA chip includes 20 OpAmps [11]). The chip, with an area of 5

x 7 mm^2 was manufactured through TSMC, in 0.18u feature size for 1.8V.

Figure 2 provides the block diagram of the standard cell and illustrates some of the more interesting features, with the reconfigurable circuitry at its core. It includes two re-configurable resistances, R1 and R2, in parallel with the capacitors C1 and C2 respectively. Each RC set can be by-passed through a switch. When the reconfigurable circuitry is programmed as an operational amplifier, the "external" resistances and capacitors allow the implementation of inverting amplifiers, integrators, differentiators, etc. The reconfigurable resistances R1 and R2 allow programmable flexibility in any configured OpAmp based circuit, and can be programmed to assume the following values: 1.8k, 6k, 9k and 18kΩ. Four switches control the resistor value. The capacitors C1 and C2 have values of 100fF. An analog memory is also included in the cell.

Figure 3 shows the details of the reconfigurable circuitry, consisting of 14 transistors connected through 44 switches. The re-configurable circuitry is able to implement different building blocks for analog processing, such as two and three stages OpAmps, logarithmic photodetectors, or Gaussian computational circuits. It includes three capacitors, Cm1, Cm2 and Cc, of 100fF, 100fF and 5pF respectively.

3. Lessons Learned

As in any design, a lot can be said about trade-offs of different conflicting constraints. The flexibility given by freedom in interconnectivity increased the number of switches and, ultimately, die size. Rapid reconfiguration required increasing the size of the internal buses that need to go to every cell, also greatly increasing the area. Additionally, the transition from the FPTA1 to the FPTA2 involved a change in technology, the HP 0.5u being replaced by the TSMC 0.18u. This change led to an increased time for layout, since we had to re-design our library. Nevertheless, it allowed the integration of a larger number of cells in a smaller die area. The capacitors' sizes were also a determining factor that contributed to the total chip area, and we had to limit their sizes to a maximum of 5pF per cell. Nevertheless, the adequate positioning of these capacitors within the cell may allow the exploration of the Miller effect, increasing the equivalent value of the capacitor. In the case of the first chips, an external output buffer had to be included whenever a capacitive load of values higher than around 50pF had to be driven. In the FPTA2, the third stage of the re-configurable circuitry (Figure 3) can optionally work as an on-chip output buffer.

Finally, we were also able to improve the logic interface, by allowing partial chip re-configuration and include latches before the analog switches to avoid transient effects during the cell re-configuration.

4. Conclusion

The paper presents a second generation evolution-oriented device, with a high level of integration, incorporation of programmable resistors, capacitors, and a (vision) sensor array, realizing in fact a first evolvable sensor system on a chip.

Acknowledgements

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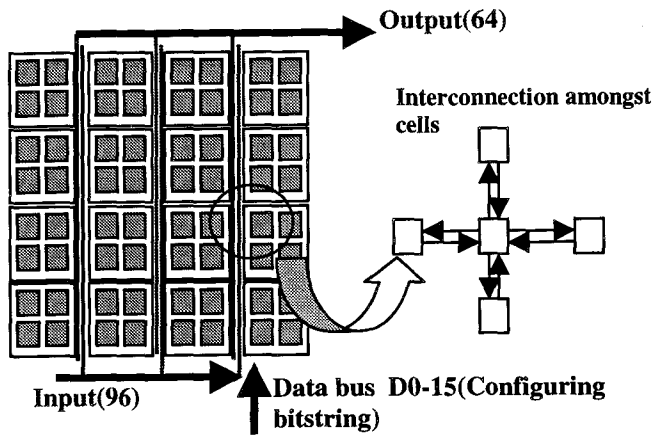

Figure 1 – Architecture of the FPTA2.

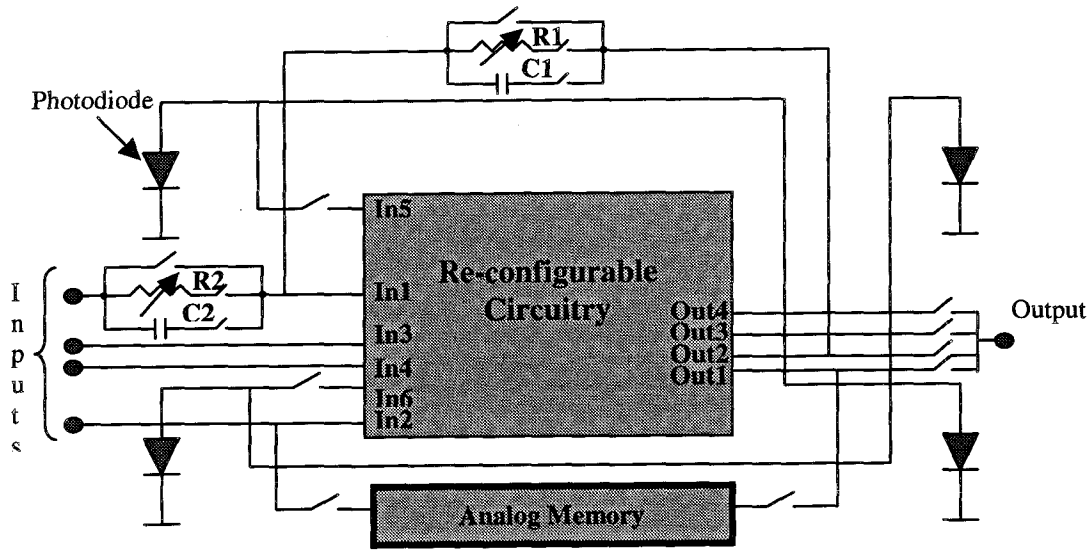

Figure 2 – Block diagram of the cell.

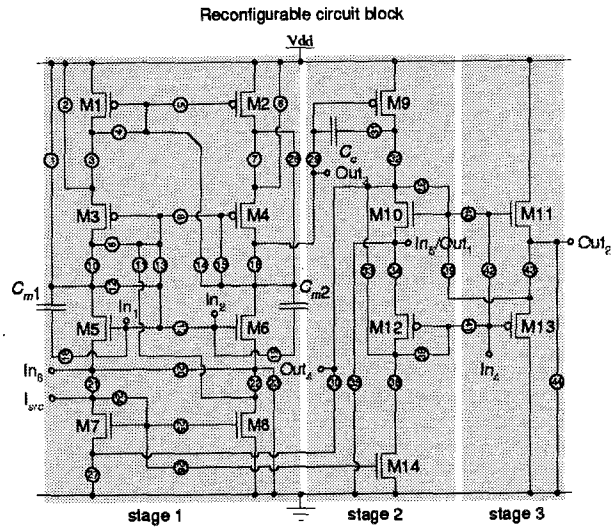

Figure 3 – Re-configurable circuitry. Switches are represented by circles.